Software Defined Radio for Covert COMMS, Signal Analysis and Direction Finding

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Abstract

Software Defined Radio (SDR) development has greatly benefited from the introduction of highly integrated, programmable transceivers offered by Analog Devices (ADI), Texas Instruments (TI) and others. Vanteon's most recent SDR, vProtean, is based on the Analog Devices ADRV9002 highly integrated, wideband, RF transceiver and the Xilinx Zynq-7020 All Programmable System-on-Chip (SoC). The ADRV9002 is coupled with a custom designed RF front end which enables operation over the full frequency range of the ADRV9002. Together, these components create a flexible, cost-effective and highly integrated SDR platform that balances size, weight, performance and power dissipation. Vanteon has fielded signal analyzers, direction finders and communication solutions using our SDR technology. We are currently engaged on several projects specifically employing our vProtean SDR technology on next generation, fielded solutions.

Introduction

Software Defined Radio is a concept derived from the technological goal of having one hardware platform which can be modified, reprogrammed and restructured to effect most any radio configuration of interest to 1) communicate voice, data, video, etc. while keeping the communications robust, jamming resilient and secure, 2) sense the RF environment to detect other communications, and 3) aid in Direction Finding (DF) of transmitters when receivers are phase coherently ganged. Historically, SDRs began as rack mounted systems to realize a flexible and scalable architecture which could be frequency agile, use arbitrary modulations and implement frequency and bandwidth adaptable filters, among other features, and have progressed toward smaller form factors. Most recently, highly integrated ASICs have facilitated development of RF to microwave frequency SDRs which have excellent size, weight, dissipated power, cost and communication performance metrics. Vanteon Corporation has been a leader in the implementation of these latest transceivers and, as a complementary technology, Field Programmable Gate Array (FPGA) System-on-Chip (SoC) which facilitates an efficient, baseband waveform processor, a radio controller, a communications hub and reconfigurability. Our vProtean SDR Platform was expressly developed with these objectives in mind.

There are several benefits related to adopting SDR technology. SDRs are flexible through their reprogrammability, so they can be cost-effectively modified, as there is no reason to physically modify the hardware in order to change the functionality. Within certain constraints, one common hardware platform can provide the functionality of multiple radios, which reduces the number of fielded radios and, most significantly, the logistics of maintenance, spare parts and batteries. Additionally, Non-Recurring Engineering (NRE) of software and firmware development can be leveraged across radio variants and repurposed for use on novel radio products, which reduces development time and costs. A revision to the SDR's functions and features can be fielded by simply changing its software and firmware, often Over-the-Air (OTA), thus reducing maintenance and implementation costs. Lastly, SDR platforms reduce time-to-market for supporting new and emerging standards, operational conditions and situational requirements, since new hardware does not have to be designed, developed, tested, certified and fielded.

The flexibility of an SDR comes from its ability to be reprogrammed, that is, the ability to change its software and firmware that defines how it works. All SDRs use one or more microprocessors, FPGAs, and/or Digital Signal Processors (DSP) and/or Graphical Processing Units (GPU) that are easily reprogrammed. Vanteon's experience with FPGAs has allowed us to achieve a significant advantage by utilizing FPGA/microprocessor SoCs to realize a capable SDR which is power efficient and has a small form factor while maintaining a manageable thermal dissipation. Our approach has consistently been to reconsider how the DSP algorithms, communication and control blocks should be implemented and decide which are best allocated to the Programmable Logic (PL) of the FPGA or to the microprocessor. Using this approach, we are able to match FPGA SoCs to the application to achieve both a capable solution and minimize power dissipation, size and cost. Typically, the DSP algorithms are instantiated into the PL of the FPGA, though not always. Later, we'll describe the MATLAB/Simulink flow we use for simulation of the signal processing, the generation of the Hardware Description Language (HDL), and the writing of the software.

vProtean SDR Technology

Vanteon's vProtean Platform is an SDR platform (Figure 1) that is well suited for a variety of markets, including government, industrial, and medical, due to its high integration, adaptable dual-transceivers, good narrowband (12 kHz) performance and lower fielded cost than alternative SDR solutions. It is based on the Analog Devices' ADRV9002, a highly integrated RF transceiver. This device supports instantaneous bandwidths between 12 kHz and 40 MHz and has a broad operational RF frequency range from 30 MHz to 6 GHz. The ADRV9002 has dual transceiver channels and provides support for 2x2 MIMO, integrated DPD, FDD or TDD in a single package. Features also include low power consumption and fast locking for frequency hopping support. Additionally, the dual transceiver channels may be phased locked to achieve an 80 MHz bonded bandwidth which may be useful for signal analysis applications.

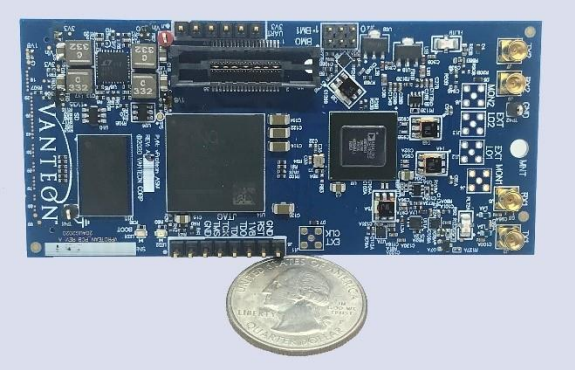

Figure 1: vProtean Platform SDR

Vanteon has paired the ADRV9002 with Xilinx's Zynq-7020 All Programmable System-on-Chip (SoC). The Xilinx 7000 family of SoCs offers high-speed Programmable Logic (PL) and Cortex-A9 ARM processors and the Zynq-7020 offers a reasonable compromise of FPGA resources, dual Cortex-A9 ARM processors, dissipated power and component pricing. Additionally, other Zynq devices in the family are targeted to

either add resources or reduce cost. Appropriately for each design, the algorithms, control and communication blocks are tailored and partitioned between the Programmable Logic (PL) and ARM cores. For the vProtean, the Zynq-7020 provides for instantiation into PL of DSP algorithms such as a highly paralleled, multi-channel receiver architecture which enables either non-blocking reception of uniquely coded, simultaneously transmitted signals or a paralleled Fast Fourier Transforms (FFT) to expedite signal analysis. Additionally, the non-blocking, multi-channel receiver architecture adapts to a wide variety of environments where interfering signals may be present, or where frequency hopping may be desired.

Additionally, Vanteon has developed and offers many Digital Signal Processing (DSP) soft core modules that target the programmable logic in the Zynq-7000 series FPGA, or similar. These DSP modules provide various processing techniques such as modulation/demodulation, digital down/up conversion, symbol timing recovery and tracking, carrier recovery and tracking, digital filters, automatic gain control, channel coding, multi-channel transmitters and receivers, forward error correction (FEC) techniques and spread spectrum coding. Examples of the modulation/demodulation techniques available include ASK/AM, FSK/FM, PSK/PM, QAM, OFDM and pseudo-noise waveforms. Some of the digital filters available include FIR, IIR, multi-rate, and adaptive filtering. Lastly, an Ethernet interface is implemented on the vProtean for host communications.

The vProtean Platform was conceived with size, weight, power and cost in mind. To maximize utilization and minimize the required Zynq size, the baseband processing, including the waveform processing, ADRV9002 control, data management etc., are segregated between the PL and the two hard-core ARM processors. The distinct functional blocks are modeled in the MATLAB/Simulink flow to simulate the waveform functions. Once the DSP functions are verified, the MATLAB modules are synthesized into HDL. The HDL representations are then incorporated into a Vivado project, along with the ARM firmware, and instantiated into the Zynq FPGA.

The mechanical design achieves a small, volumetric space (28.8 cm^3) with a low-profile, high density, digital signal connector enabling mount as a daughter card. All RF ports are MMCX connections. Figure 2 shows the backside of the vProtean and the 100-pin connector. Additionally, a Carrier Board was designed to permit testing the vProtean using standard interfaces, e.g. Ethernet, JTAG, USB, microSD card etc. See Figure 3 showing the vProtean mounted on the Carrier Board.

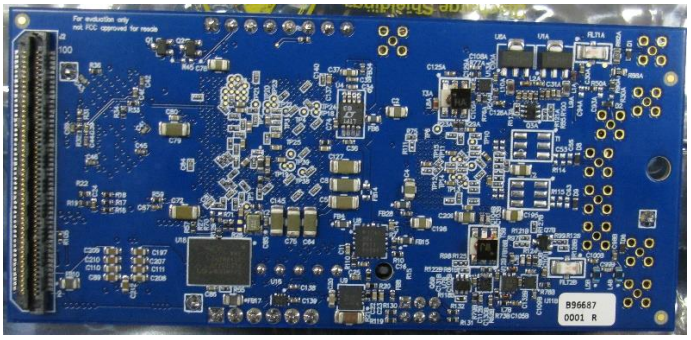

Figure 2: Bottom Side of vProtean Platform SDR

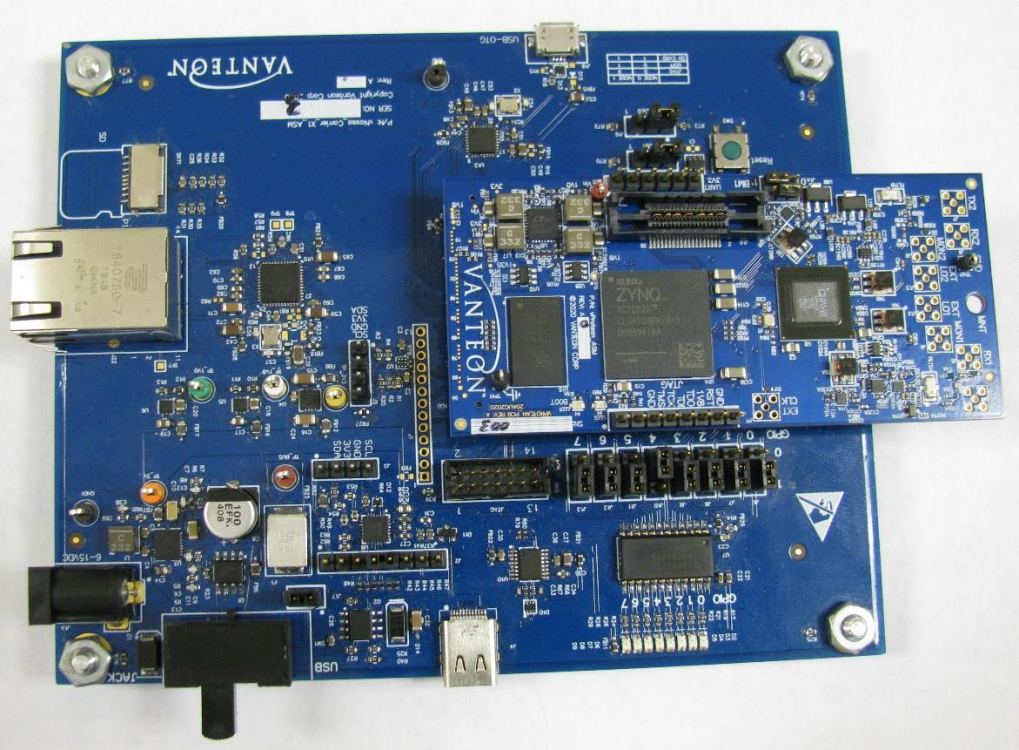

Figure 3: vProtean on Carrier Board having Ethernet, JTAG, USB, microSD Card and other connections

vProtean Target Applications

The Vanteon vProtean SDR has a native, operational frequency of 30 MHz to 6000 MHz, which can be extended to Ka-band using block up/down converters. Its transmitter synthesis bandwidth and receiver bandwidth range are 12 kHz to 40 MHz and channels may be phased-locked to effect a broader, bonded bandwidth for signal analysis of spectrum wider than 40 MHz. Additionally, the integrated Digital Predistortion (DPD) capabilities of the ADRV9002 benefit applications requiring efficient transmitters when using high Peak-to-Average Power Ratio (PAPR) envelope waveforms. The higher efficiency enhances battery life when using, for example, OFDM and QAM like modulations.

The fast frequency locking capabilities of the ADRV9002 make the vProtean an excellent, frequency hopping, communications radio which are used in current designs to achieve interference avoidance, communication robustness and low probability of detection. Hundreds of narrowband channels can be implemented in the 40 MHz full bandwidth mode with practically instantaneous switching times (i.e. digitally). Up to 64 channels can be preprogrammed (outside the 40 MHz bandwidth) into a fast frequency hopping table to obtain very fast (~20 uS) switching times. Additionally, an arbitrary frequency hopping mode is supported, albeit with a greater transition time between frequencies.

Additionally, coupling fast frequency hopping with vProtean's arbitrary waveform modulation capabilities, enabled by the Xilinx Zynq-7020 SoC, allows many standard modulation protocols, i.e.

OFDM, and, of more interest, non-standard modulations that exploit the weaknesses of fielded surveillance systems to lower the chance of detection.

Lastly, the ability to reprogram the vProtean, FPGA PL and ARM firmware, on the fly, permits swapping modes from a communications radio to a capable signal analyzer and/or DF receiver function. This is dependent on the antenna configuration, and we note that an antenna configuration which optimizes DF functionality could alternately be used for communications.

Current Status

Vanteon is simultaneously designing for multiple clients' communication radios, signal analyzers and DF receivers, while working to fully characterize the RF performance. We have demonstrated the full functionality of a communications radio, and the receiver for signal analysis and DF. Unfortunately, we will be later than the submission date for this RFS when we have quantitatively measured performance parameters. These are measurements made to date.

Parameter	Typical	Units
Transmitter Center Frequency	30 - 6000	MHz
Transmit Power (P1dB)	18	dBm
Transmitter Synthesis Bandwidth	0.012 - 40	MHz
Receiver Center Frequency	30 - 6000	MHz
Maximum Gain	32	dB
Noise Figure	3.5	dB

Qualitatively, vProtean is matching the anticipated performance parameters as defined by the ADI ADRV9002 (https://www.analog.com/media/en/technical-documentation/data-sheets/adrv9002.pdf).

Development Schedule

Vanteon is actively engaged in design and development of three projects leveraging our SDR architecture.

1. Low Probability of Detection COMMS Radio - Demonstration of key features and performance is scheduled for March 2021. First articles of field ready unit scheduled for early 2021.
2. Broadband Spectrum and Signal Analyzer - Prototype characterization in progress. Initial integration with our client's system in progress. First articles of field ready unit scheduled for August 2021.
3. Cellular Transmission Detector - Simulation in MATLAB/Simulink complete. Writing HDL and C++ for prototype initial testing.

Additionally, we have quoted on an OTA project and a DARPA project which would use the vProtean as a transceiver module.

Conclusion

Vanteon Corporation has applied Software Defined Radio technology to a variety of unique applications in which size, weight, power and performance were all important requirements. Analog Device's ADRV9002 has enabled a very capable SDR development with direct application to military communications, low detectability communications, signal analysis for transmission detection, and direction finding of transmitters. We are actively engaged in several projects making these systems a reality and are actively seeking other opportunities to exploit this technology.

Vanteon Background

Vanteon is an electronic solutions, design and engineering consulting firm, specializing in collaborative design, development and sustaining engineering for electronic hardware and software products. Vanteon has more than 35 years of experience in developing next-generation solutions with emphasis on RF/Microwave sub-systems, Software Defined Radio, embedded hardware/firmware, and software development.